Mail Stop Appeal Brief - Patents

PATENT Attorney Docket No. MTI-31529

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant	:	Ronald A. Weimer
Serial No.	:	09/935,255
Filing Date	:	August 22, 2001
For	:	Method of Composite Gate Formation
Group Art Unit:		2893
Examiner	:	CHEN, Jack S. J.
Confirmation No.:		1208

CERTIFICATION OF SUBMISSION

I hereby certify that, on the date shown below, this correspondence is being transmitted via the Patent Electronic Filing System (EFS) at the U.S. Patent and Trademark Office.

Date: 10-12-2009 Jill K. Robinette

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Sir:

This is an appeal from the final rejection of Claims 1-5, 7-14, 16-21, 98-100, 103-106 and 112, as stated in the Office Action mailed June 10, 2009.

A Notice of Appeal was filed August 10, 2009.

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I. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

There is a pending appeal for related application U.S. Serial No. 10/932,130 (Appeal Brief filed June 19, 2009).

Appellant's legal counsel: Kristine M. Strodthoff, Reg. No. 34,259, Whyte Hirschboeck Dudek S.C.

Assignee: Micron Technology, Inc.

III. STATUS OF CLAIMS

All the claims of this application and their individual status are as follows. A copy of the claims involved in the appeal is provided in the Claims Appendix.

Claims pending: 1-5, 7-57, 73, 75-81, 96 and 98-121

Claims canceled: 6, 58-72, 74, 82 and 97

Claims withdrawn from further consideration: 15, 22-57, 73, 75-81, 83-96, 101, 102, 107-111 and 113-121

Claims on appeal: 1-5, 7-14, 16-21, 98-100, 103-106 and 112

IV. STATUS OF AMENDMENTS

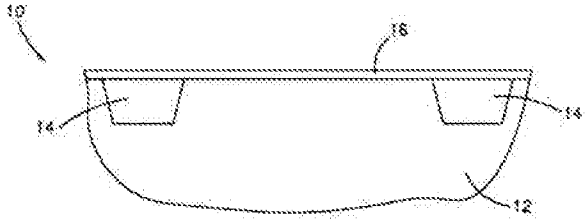
All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

All of the claims under appeal are drawn to various embodiments of a method of forming a silicon nitride barrier layer that is effective to inhibit passage of a dopant into an underlying dielectric/oxide material.

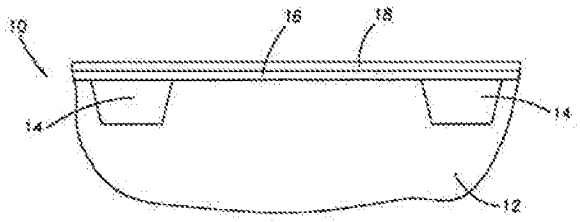
The independent claims under appeal are 1, 5, 7-9 and 16-20.

Appellant illustrates the claimed method of forming a silicon nitride barrier layer in Figs. 1-3 (shown below), which is described in the specification at pages 5-7.



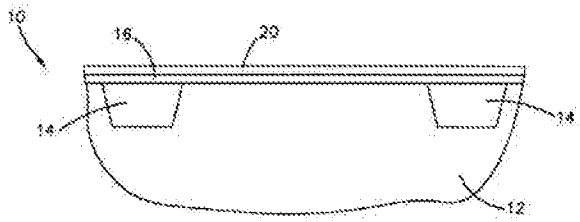
⇐ ***dielectric/gate oxide* 16**

FIG. 1



⇐ ***silicon layer* 18**

FIG. 2



⇐ ***silicon nitride barrier layer* 20**

FIG. 3

Appellant's method is distinguished from the cited prior art by the formation of a continuous silicon layer (**18**) over the dielectric material (**16**) – and a silicon nitride layer (**20**) that is an effective dopant barrier.

Regarding Claim 1, the method is illustrated in **Figs. 1-3** (shown above) and described in the specification at pages 6-7. The dielectric material (**16**) is exposed to a silicon gas under low partial pressure to deposit a continuous silicon layer (**18**) over the dielectric material, which is then exposed to a nitrogen gas to nitridize the silicon layer (**18**) and form a silicon nitride barrier layer (**20**) that is effective to inhibit passage of a dopant into the underlying dielectric material (**16**).

Formation of the silicon layer (**18**) is illustrated in **Fig. 2** and described at page 6, line 15 to page 7, line 2. The formation of the silicon layer (**18**) as a 'continuous' layer is illustrated in **Fig. 2** and described at page 6, lines 15-22 (see also, the further discussion below with regard to the Section 112(1) rejection).

Nitridizing the silicon layer (**18**) to form a silicon nitride barrier layer (**20**) is illustrated in **Fig. 3** and described at page 7, lines 3-22. The silicon nitride layer (**20**) as a barrier to inhibit passage of dopants (e.g., boron) is described at page 7, lines 23-24, and in Claims 53-54 as originally filed.

Claim 5 recites the elements of Claim 1 with the exception of the terms 'irradiating' (page 6, line 15) with a silicon gas to 'nucleate' (page 16, line 16) the dielectric material with silicon, and exposing the silicon layer to nitrogen gas to 'form' a silicon nitride barrier layer.

Claim 7 recites the elements of Claim 1, with the exception of 'nitridizing' the silicon layer (page 7, line 3).

Claim 8 recites the elements of Claim 1, with the exception of exposing a 'surface' (page 6, line 17) of the dielectric material to silicon gas to 'nucleate' (page 16, line 16) the surface of the dielectric material.

Claim 9 recites the elements of Claim 7, with the additional limitation of a partial pressure of about 10^{-2} Torr or less as described at page 6, line 28, and with the exception of 'nitridizing the silicon layer' (without reciting a nitrogen gas).

Claim 16 recites elements of Claim 8 and 9, with the exception of a limitation of a partial pressure range of about 10^{-2} to 10^{-7} Torr (page 6, lines 28-29) to 'nucleate' (page 16, line 16) the dielectric layer.

Claim 17 recites the elements of Claim 16 with the additional limitations of temperature and duration of exposing the dielectric material to the silicon gas, as described at page 6, line 28 to page 7, line 2.

Claim 18 recites the elements of Claim 7, with the exception of limitation of 'thermal annealing' the silicon layer in nitrogen gas, as described at page 2, line 27 and page 3, lines 8 and 16.

Claim 19 recites the elements of Claim 1, with the additional limitation of exposing the silicon layer to nitrogen gas at a 700-900°C, as described at page 7, line 12.

Claim 20 recites the elements of Claim 19, with the additional limitations of pressure, flow rate and duration, as described at page 7, lines 12-13.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether Claims 1-5, 7-14, 16-21, 98-100, 103-106 and 112 fail to comply with the written description requirement (lack of enablement) under 35 U.S.C. §112, first paragraph.

2. Whether Claims 1-5, 7-14, 16-19, 98-100, 103-104, 106 and 112 are unpatentable under 35 USC §102(e) as being anticipated by Muralidhar (USP 6,297,095).

3. Whether Claims 20-21 and 105 are unpatentable under 35 USC §103(a) as being obvious over Muralidhar (USP 6,297,095).

VII. ARGUMENT

1. Whether Claims 1-5, 7-14, 16-21, 98-100, 103-106 and 112 fail to comply with the written description requirement (lack of enablement) under 35 U.S.C. §112(1).

The Examiner finally rejected Claims 1-5, 7-14, 16-21, 98-100, 103-106 and 112 under 35 U.S.C. § 112, first paragraph, on the basis that the term 'continuous' is not described/supported in the specification as originally filed.

In the final Office Action (mailed June 10, 2009) at page 2, the Examiner stated as follows (emphasis in the original):

> Re claims 1, 5, 7, 8, 9, 16 and 17, the phrase *"continuous* layer of silicon" and/or *"continuous* silicon nitride barrier layer" was not described/supported by the original specification.
>
> Re claims 18, 19 and 20, the phrase *"continuous* silicon layer" was not described/supported by the original specification.

It is clear from Appellant's description and figures, that the silicon material is formed as a layer that is *continuous* over the dielectric/oxide layer.

The specification provides processing conditions and methods for forming the silicon material – and describes the silicon material as being deposited *as a layer* pointing to *layer 18* in **FIG. 2**.

See **FIG. 2** (below) and the specification at page 6, line 15 to page 7, line 2, and particularly page 6, lines 15-26 as follows: (emphasis added).

> According to the invention, the gate oxide layer [16] is irradiated with a silicon-containing species under low partial pressure, high vacuum conditions *to deposit (nucleate) a thin layer 18 of silicon* onto the surface [~~16~~] of the gate oxide layer [16], ***as shown in FIG. 2***. The silicon layer can comprise polysilicon or amorphous silicon. The processing conditions results in a *silicon layer 18* that is thinner than can be achieved under standard silicon growth conditions, i.e., a temperature greater than 600°C., and a pressure greater than 100 mTorr, with SiH_2, Si_2H_7, or dichlorosilane (DCS, SiH_2Cl_2). Preferably, the silicon layer 18 is less than about 30 angstroms, preferably about 10 to about 20 angstroms thick. Exemplary silicon source materials include SiH_2Cl_2, silicon tetrachloride ($SiCl_4$), and a silicon that contains a hydride such as silane (SiH_4), and disilane (Si_2H_6). *The silicon material can be deposited as a layer* utilizing any known deposition process including plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), and rapid thermal chemical vapor deposition (RTCVD).

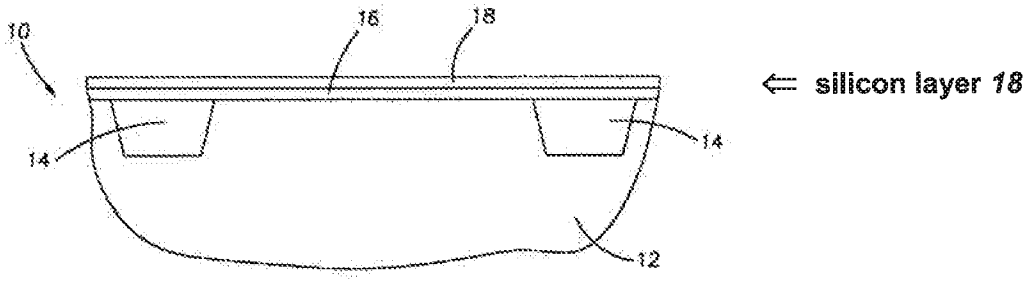


FIG. 2

FIG. 2 clearly illustrates the silicon material layer **18** as a *continuous* layer over the surface of the underlying dielectric (oxide) layer **16**. Based on Appellant's disclosure, the nature of a continuous layer formed by Appellant's method is not ambiguous to one skilled in the odorants arts and would be readily ascertainable.

It is respectfully submitted that the term 'continuous' layer of silicon in the claims is sufficiently described in the specification and figures as originally filed, which are more than adequate to enable one of ordinary skill in this art area to carry out the invention commensurate with the scope of claims, as required under Section 112(1).

Based on Appellant's disclosure and the understanding in the art, it is submitted that the requirements under Section 112(1) have clearly been met in the present disclosure, and that an art worker in this area is fully enabled to practice Appellant's invention as claimed.

Accordingly, withdrawal of this rejection is respectfully requested.

2. Whether Claims 1-5, 7-14, 16-19, 98-100, 103-104, 106 and 112 are unpatentable under 35 USC §102(e) as being anticipated by Muralidhar (USP 6,297,095).

The Examiner finally rejected Claims 1-5, 7-14, 16-19, 98-100, 103-104, 106 and 112 under 35 U.S.C. § 102(e) as anticipated by Muralidhar (USP 6,297,095).

To anticipate, a single reference must disclose each and every limitation of the claimed invention. *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir. 2006); *Eolas Technologies Inc. v. Microsoft Corp.*, 73 USPQ2d 1782 (Fed. Cir. 2005).

The rejection is in error because Muralidhar fails to teach or suggest:

a) Forming a *continuous* silicon layer on a dielectric (oxide) material, and/or

b) Nitridizing the silicon layer to form a *silicon nitride barrier layer* that is *effective to inhibit passage of a dopant therethrough* to the underlying dielectric material.

In the final Office Action (mailed June 10, 2009), the Examiner stated as follows (page 3; paragraph 2; emphasis added):

> Re claim 1, Muralidhar discloses a method of forming a nitride barrier layer, comprising the steps of: exposing a dielectric material 14/102 to a silicon-containing gas under low partial pressure **to deposit a continuous layer of silicon 15/16/17/18/19/21/103/104 (figs. 6-10, 21-22, col. 10, lines 25-65;** note: **the continuous layer is comprising of a plurality of uniform nanoclusters** that were formed across the surface of the tunnel dielectric layer 14/102; further in this regard, ***each of the nanoclusters can also be considered as a continuous layer)*** *over the dielectric material;* ...see figs. 1-28 and cols. 1-22 for more details.

Continuous Silicon Layer. In Muralidhar, the Examiner cites particularly to ***nuclei 15/16/17*** in Figs. 6-7, to ***nanoclusters 18/19/21*** in Figs. 8-10, and ***nanoclusters 103/104*** in Figs. 21-22, as teaching a *'continuous' silicon layer*. These figures are shown below.

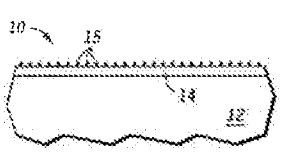


FIG.6

(*nuclei* 15)

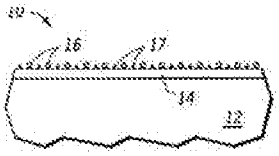


FIG.7

(*nuclei* 16/17)

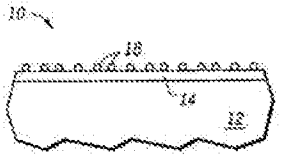


FIG.8

(*nanoclusters* 18)

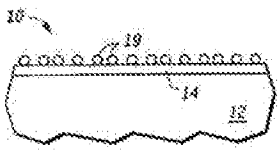


FIG.9

(*nanoclusters* 19

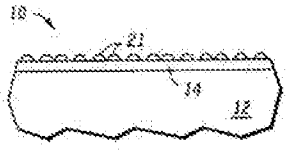


FIG.10

(*nanoclusters* 21)

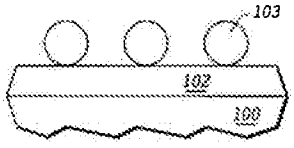


FIG.21

(*nanoclusters* 103)

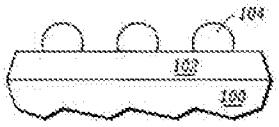


FIG.22

(*nanoclusters* 104)

In each of these structures, the dielectric layer **102** is *exposed* between the spaced apart nuclei/nanoclusters. *None* of these structures provides a 'continuous' silicon layer over the dielectric/oxide layer **102**.

In Muralidhar's discussion of the formation of nanoclusters in the Background section, the patentee stresses the *importance* of *controlling the spacing between* the nanoclusters. See at col. 2, lines 5-24 (emphasis added).

> In order to reduce the required thickness of the tunnel dielectric and improve the area efficiency of the memory structures by reducing the need for charge pumps, *the uniform layer of material used for the floating gate may* be *replaced with a plurality of nanoclusters, which operate as isolated charge storage elements.* ...In combination, *the plurality of nanoclusters provide adequate charge storage capacity* ***while remaining physically isolated from each other*** such that any leakage occurring with respect to a single nanoclusters via a local underlying defect does not cause charge to be drained from other nanoclusters (***by controlling average spacing between nanoclusters***, *it can be ensured that there is no lateral charge flow between nanoclusters in the floating gate*). As such, thinner tunnel dielectrics can be used in these device structures. ...

In the Detailed Description, Muralidhar further teaches that the silicon nanoclusters are *isolated* and *spaced apart* – to avoid lateral charge transfer between nanoclusters. See at col. 12, lines 50-67 (emphasis added)

> ...In such an embodiment, *the coverage,* or area density of the nanoclusters on the underlying tunnel dielectric layer *may be approximately 20%.* The 20% area density is reasonable for semiconductor device manufacturing, *as it provides a level of tolerance* ***in the spacing between the nanoclusters*** included in the floating gate structures. Although higher area densities may be achieved, the proximity of the isolated storage elements in such higher area density embodiments may increase the probability of lateral charge transfer between nanoclusters, thus degrading the ***beneficial effects of their isolation***.

Clearly, Muralidhar does *not* teach or suggest forming a *continuous* silicon layer over a dielectric material as defined in Appellant's claims.

As such, Muralidhar cannot anticipate the claims.

Barrier Layer. Furthermore, Muralidhar does not teach or suggest forming a *silicon nitride barrier layer effective to inhibit passage of a dopant* therethrough to an underlying dielectric material.

First of all, in the embodiment shown in **Fig. 23** below, a nitride layer **106** is formed only on the silicon nanoclusters **104**. The dielectric layer **102** between the nanoclusters is *exposed* and *not* nitrided. This is stated by Muralidhar at col. 16, lines 55-67 (emphasis added).

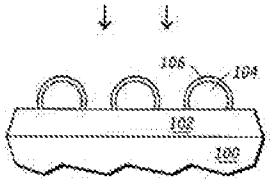


FIG.23

Typically, the *nitriding ambient* used for forming the encapsulation layer **106** *does not affect the underlying tunnel dielectric layer* ***102*** in a significant manner. As such, the nitriding step utilized to form the encapsulation layer **106** *will not result in nitridation of the underlying tunnel dielectric layer* ***102***. As such, *traps* that may be generated within the encapsulation layer **106** *are isolated from the underlying substrate* ***100*** *as well as from the encapsulation layers of neighboring nanoclusters.* As such, *trap assisted leakage between the nanoclusters is less likely to occur.* This lack of degradation of charges stored in the traps may actually enhance the charge storage characteristics of the nanoclusters **104**.

In another embodiment shown in **Fig. 25** below, a nitride layer **107** is formed by *deposition – not nitridation* as defined in the claims. See at col. 17, lines 13-18 (emphasis added).

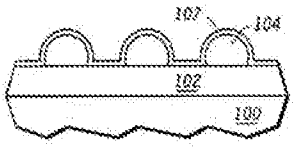


FIG.25

In other embodiments, a protecting nitride layer may be ***deposited rather than grown*** on individual nanoclusters. **FIG. 25** illustrates the *nanocluster structures* as shown in FIG. 22 following a step where a thin nitride layer **107** is *deposited*. The nitride layer **107** *may be deposited using CVD operations* that utilize ammonia and dichlorosilane. Such CVD operations may be performed using LPCVD or UHVCVD techniques. ...

Secondly, the nitride layers **106/107** are only taught as a barrier to *oxygen* – *not* as a dopant barrier. This is stated by Muralidhar at col. 17, lines 1-12 and 28-40 (emphasis added).

> ...By including the encapsulation layer **106**, *oxidation* or other degradation *due to oxidizing ambient exposure* of the nanoclusters **104** can be reduced or eliminated. As such, the diameter of the nanoclusters **104** is maintained, and no uncontrolled increase in the underlying tunnel dielectric occurs.
>
> ...
>
> The thin nitride layer **107** illustrated in **FIG. 25** forms a *barrier to oxygen* such that both the nanoclusters **104** and the underlying semiconductor substrate **100** below the tunnel dielectric layer **102** are *protected from oxidation*. As such, the potential for an increase in the thickness of the tunnel dielectric layer **102** is reduced.

There is no teaching in Muralidhar of a dopant barrier.

In sum, the Examiner has erroneously a) disregarded Appellant's support for the term 'continuous' in the claims, and b) mischaracterized and ignored the express teachings of Muralidhar.

Muralidhar does not teach or suggest forming a *continuous* silicon layer on a dielectric material and/or nitridizing the silicon layer to form a silicon nitride *barrier layer* that is effective to inhibit passage of a *dopant* therethrough to the underlying dielectric material, as defined in the claims.

Accordingly, withdrawal of this rejection is respectfully requested.

3. Whether Claims 20-21 and 105 are unpatentable under 35 USC §103(a) as being obvious over Muralidhar (USP 6,297,095).

In the final Office Action (mailed June 10, 2009), the Examiner finally rejected Claims 20-21 and 105 under 35 U.S.C. § 103(a) as obvious over Muralidhar (USP 6,297,095).

Independent Claim 20 recites the elements of Claim 1 – with the addition of processing parameters for exposing the silicon layer to a nitrogen gas (i.e., process temperature, pressure, flow rate, time). Claim 21 depends from independent Claim 20, and defines the nitrogen-containing gas.

Claim 105 depends from Claim 1 and defines exposing the silicon layer to a nitrogen gas according to the temperature, pressure and flow rate.

The Examiner maintains that, although Muralidhar is silent regarding the flow rate and duration of nitrogen gas, the use of the defined ranges would be obvious and, as such, Claims 20-21 and 105 are obvious based on Muralidhar's disclosure.

The rejection is in error because, as discussed hereinabove, there is no teaching or suggestion in Muralidhar of:

a) Forming a *continuous* silicon layer on a dielectric material, and/or

b) Nitridizing the silicon layer to form a silicon nitride *barrier layer* that is effective to inhibit passage of a *dopant* therethrough to the underlying dielectric material.

As such, the Examiner has failed to establish a case of *prima facie* obviousness of Appellant's methods as defined in any of Claims 20-21 and 105 based on Muralidhar's disclosure. Accordingly, withdrawal of this rejection is respectfully requested.

Extension of Term.

The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Appellant believes that no extension of term is required, but conditionally petitions for an extension of time if so required. If any extension and/or fee are required, please charge Account No. 23-2053.

For the reasons stated in the above arguments, Appellant believes that the claims on appeal comply with 35 U.S.C. §112(1) and §§ 102/103, and requests that the final rejection of the claims on appeal be reversed.

Respectfully submitted,

Kristine M. Strodthoff

Dated: October 12, 2009

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VIII. CLAIMS APPENDIX

The claims on appeal are:

1. A method of forming a nitride barrier layer, comprising:

exposing a dielectric material to a silicon-containing gas under low partial pressure to deposit a continuous layer of silicon over the dielectric material; and

exposing the silicon layer to a nitrogen-containing gas to nitridize the silicon layer to form a continuous silicon nitride barrier layer effective to inhibit passage of a dopant into the dielectric material.

2. The method of Claim 1, wherein the dielectric material is exposed to the silicon-containing gas at a partial pressure of about 10^{-2} Torr or less.

3. The method of Claim 1, wherein the dielectric material is exposed to the silicon-containing gas at pressure of about 10^{-2} to about 10^{-7} Torr.

4. The method of Claim 2, wherein the dielectric material is exposed to the silicon-containing gas at a temperature of about 500°C to about 700°C.

5. A method of forming a nitride barrier layer, comprising:

irradiating a dielectric material with a silicon-containing gas under low partial pressure to nucleate the dielectric material with a continuous layer of silicon; and

exposing the silicon layer to a nitrogen-containing gas to form a continuous silicon nitride barrier layer effective to inhibit passage of a dopant into the dielectric material.

7. A method of forming a nitride barrier layer, comprising:

exposing a dielectric material to a silicon-containing gas under low partial pressure to deposit a continuous layer of silicon over the dielectric material; and

nitridizing the silicon layer in a nitrogen-containing gas to form a continuous silicon nitride barrier layer effective to inhibit passage of a dopant into the dielectric material.

8. A method of forming a nitride barrier layer, comprising:

exposing a surface of a dielectric material to a silicon-containing gas at a low partial pressure to nucleate the surface of the dielectric material and form a continuous layer of silicon thereon; and

exposing the silicon layer to a nitrogen-containing gas to form a continuous silicon nitride barrier layer effective to inhibit passage of a dopant into the dielectric material.

9. A method of forming a nitride barrier layer, comprising:

exposing a dielectric material to a silicon-containing gas at a partial pressure of about 10^{-2} Torr or less to deposit a continuous layer of silicon thereon; and

nitridizing the silicon layer to form a continuous silicon nitride barrier layer effective to inhibit passage of a dopant into the dielectric material.

10. The method of Claim 9, wherein the dielectric material is exposed to the silicon-containing gas at a temperature of about 500°C to about 700°C.

11. The method of Claim 9, wherein the silicon-containing gas is selected from the group consisting of dichlorosilane, silicon tetrachloride, silane, and disilane.

12. The method of Claim 9, wherein exposing the dielectric material to the silicon-containing gas is by plasma enhanced chemical vapor deposition, low pressure chemical vapor deposition, or rapid thermal chemical vapor deposition.

13. The method of Claim 9, wherein the silicon-containing gas is deposited by rapid thermal chemical vapor deposition at about 500°C. to about 700°C.

14. The method of Claim 9, wherein the dielectric material comprises silicon dioxide.

16. A method of forming a nitride barrier layer, comprising:

exposing a dielectric material to a silicon-containing gas at a partial pressure of about 10^{-2} to about 10^{-7} Torr to nucleate the dielectric material and form a continuous layer of silicon; and

exposing the silicon layer to a nitrogen-containing gas to form a continuous silicon nitride barrier layer effective to inhibit passage of a dopant into the dielectric material.

17. A method of forming a nitride barrier layer, comprising:

exposing a dielectric material to a silicon-containing gas at a partial pressure of about 10^{-2} to about 10^{-7} Torr, a temperature of about 500°C. to about 700°C., and a duration of about 1 second to about 5 minutes, to nucleate the dielectric material and form a continuous layer of silicon; and

exposing the silicon layer to a nitrogen-containing gas to form a continuous silicon nitride barrier layer effective to inhibit passage of a dopant into the dielectric material.

18. A method of forming a nitride barrier layer, comprising:

depositing a continuous silicon layer onto a dielectric material by exposing the dielectric material to a silicon-containing gas under low partial pressure; and

thermally annealing the silicon layer in a nitrogen-containing gas to form the nitride barrier layer, said barrier layer effective to inhibit passage of a dopant into the dielectric material.

19. A method of forming a nitride barrier layer, comprising:

depositing a continuous silicon layer onto a dielectric material by exposing the dielectric material to a silicon-containing gas under low partial pressure; and

exposing the silicon layer to a nitrogen-containing gas at a temperature of about 700°C. to about 900°C. to nitridize the silicon layer to form the nitride barrier layer, said barrier layer effective to inhibit passage of a dopant into the dielectric material.

20. A method of forming a nitride barrier layer, comprising:

depositing a continuous silicon layer onto a dielectric material by exposing the dielectric material to a silicon-containing gas under low partial pressure; and

exposing the silicon layer to a nitrogen-containing gas at a temperature of about 700°C. to about 900°C., a pressure of about 1 to about 760 Torr, and a flow rate of about 100 to about 10,000 sccm, for about 1 second to about 180 minutes to nitridize the silicon layer to form the nitride barrier layer, said barrier layer effective to inhibit passage of a dopant into the dielectric material.

21. The method of Claim 20, wherein the nitrogen-containing gas is selected from the group consisting of nitrogen, ammonia, nitrogen trifluoride, nitrogen oxide, and a nitrogen-helium mixture.

98. The method of Claim 1, wherein the silicon-containing gas is selected from the group consisting of dichlorosilane, silicon tetrachloride, silane, and disilane.

99. The method of Claim 1, wherein exposing the dielectric material to the silicon-containing gas comprises chemical vapor deposition of the silicon gas.

100. The method of Claim 1, wherein exposing the dielectric material to the silicon-containing gas comprises rapid thermal chemical vapor deposition of the silicon gas.

103. The method of Claim 1, wherein exposing the silicon layer comprises thermally annealing the silicon layer in a nitrogen-containing gas.

104. The method of Claim 1, wherein exposing the silicon layer comprises a temperature of about 700°C. to about 900°C.

105. The method of Claim 1, wherein exposing the silicon layer comprises a temperature of about 700°C. to about 900°C., a pressure of about 1 to about 760 Torr, and a flow rate of about 100 to about 10,000 sccm for about 1 second to about 180 minutes.

106. The method of Claim 1, wherein the nitrogen-containing gas is selected from the group consisting of nitrogen, ammonia, nitrogen trifluoride, nitrogen oxide, and a nitrogen-helium mixture.

112. The method of Claim 1, wherein exposing the dielectric material comprises a partial pressure of about 10^{-2} to about 10^{-7} Torr, a temperature of about 500°C. to about 700°C., and a duration of about 1 second to about 5 minutes.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.